WHAT IS CLAIMED IS:

1. A method of forming a fin field effect transistor (FinFET) device, comprising:

providing a substrate, comprising a semiconductor layer;

forming a plurality of active areas, insulated from each other by field areas, on the semiconductor layer;

forming at least one dummy gate on at least one of the active areas;

forming source and drain regions within the at least one of the active areas, the source and drain regions being self aligned to the dummy gate;

covering the substrate with an insulating layer as to leave the dummy gate exposed; and

patterning the exposed dummy gate and the semiconductor layer so as to create an open cavity in the insulating layer and in the semiconductor layer and to form a dummy fin and a semiconductor fin aligned to the dummy fin in the cavity, both of the fins extending from the source region to the drain region, thereby exposing the semiconductor layer.

2. The method of Claim 1, wherein the at least one dummy gate overlaps the at least one of the active areas.

3. The method of Claim 1, further comprising forming spacers against the sidewalls of the cavity.

4. The method of Claim 3, wherein the providing the substrate comprises forming, at least within the at least one of the active areas, a dielectric layer separating the semiconductor layer from the substrate.

5. The method of Claim 4, wherein the substrate comprises a silicon-on-insulator wafer.

6. The method of Claim 5, wherein the covering the substrate comprises:

forming the insulating layer on the substrate; and

planarizing the insulating layer until the at least one dummy gate is exposed.

7. The method of Claim 6, wherein the dummy fin comprises a stack of layers selectively removable from each other.

8. The method of Claim 7, further comprising removing at least one layer of the stack of layers.

9. The method of Claim 8, further comprising removing the remaining layers of the stack of layers.

10. The method of Claim 8, further comprising:

depositing a layer of gate dielectric and a layer of gate electrode material on the substrate; and

planarizing the layer of gate dielectric and the layer of gate electrode material until the insulating layer is exposed.

11. The method of Claim 8, further comprising:

depositing a layer of gate dielectric and a layer of gate electrode material on the substrate; and

patterning the layer of gate dielectric and the layer of gate electrode material to form a gate dielectric and a gate electrode overlapping the cavity.

12. The method of Claim 10, wherein the layer of gate dielectric comprises a layer of high-k dielectric.

13. The method of Claim 10, wherein the layer of gate electrode material comprises a metal layer.

14. The method of Claim 1, further comprising forming at least one planar FET device on an active area other than the at least one of the active areas.

15. The method of Claim 14, wherein the forming the at least one dummy gate comprises:

depositing a stack of a dielectric layer and a conductor layer; and

patterning the stack of layers to form at least one dummy gate and to form the gate of the planar FET device.

16. The method of Claim 1, wherein the dummy fin comprises at least one of an oxide layer, a polysilicon layer and a nitride layer.

17. A complementary metal-oxide semiconductor (CMOS) circuit, comprising:

at least two active areas formed in a semiconductor layer, the at least two active areas insulated from each other by field regions;

each active area comprising at least one fin field effect transistor (FinFET) device; and

each of the at least one FinFET device comprising a source and a drain formed in the semiconductor layer, and a cavity in between, with a semiconductor fin formed in the semiconductor layer and extending in the cavity from the source to the drain.

18. The CMOS circuit of Claim 17, wherein the cavity is configured to overlap the active area.

19. The CMOS circuit of Claim 18, further comprising:

an insulating oxide layer covering the CMOS circuit outside the cavity; and

spacers formed against the inner sidewalls of the cavity.

20. The CMOS circuit of Claim 18, further comprising a stack of a gate dielectric and a gate electrode overlapping the semiconductor fin.

21. The CMOS circuit of Claim 19, wherein the gate dielectric comprises a high-k dielectric.

22. The CMOS circuit of Claim 19, wherein the gate electrode comprises a metal.

23. The CMOS circuit of Claim 19, wherein the stack of a gate dielectric and a gate electrode extends beyond the cavity.

24. The CMOS circuit of Claim 19, wherein the stack of a gate dielectric and a gate electrode is coplanar with the insulating oxide.

25. The CMOS circuit of Claim 17, further comprising at least one active area comprising at least one planar FET device.

26. The CMOS circuit of Claim 17, wherein the circuit comprises a CMOS inverter.

27. A method of manufacturing a complementary metal-oxide semiconductor (CMOS) circuit, the method comprising:

providing a substrate, comprising a semiconductor layer;

forming a plurality of active areas, insulated from each other by field areas, on the semiconductor layer;

forming at least one dummy gate on at least one of the active areas;

forming source and drain regions within the at least one of the active areas, the source and drain regions being self aligned to the dummy gate;

covering the substrate with an insulating layer leaving the dummy gate exposed; and

patterning the exposed dummy gate and the semiconductor layer so as to form a dummy fin and a semiconductor fin aligned to the dummy fin, the dummy fin and the semiconductor fin extending from the source region to the drain region.

28. The method of Claim 27, wherein the patterning comprises:

patterning the exposed dummy gate so as to form the dummy fin, the dummy fin extending from the source to the drain region; and

patterning the semiconductor layer so as to form the semiconductor fin in alignment with the formed dummy fin, the semiconductor fin connecting the source and drain regions.

29. The method of Claim 27, wherein a fin field effect transistor (FinFET) device is integrated into the CMOS circuit manufacturing method.

30. The method of Claim 29, wherein the FinFET device comprises at least one of an n-type FinFET device and a p-type FinFET device.

31. The method of Claim 30, wherein the at least one of the n-type and p-type FinFET devices has a channel length of about 100 nanometer or less.

32. The method of Claim 27, wherein the dummy fin comprises at least one of an oxide layer, a polysilicon layer and a nitride layer.

33. The method of Claim 27, wherein the dummy fin comprises a plurality of layers being selectively removable from each other.